

# High Speed Front End of the Multimegabit Telemetry Demodulator Detector

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*This article presents the high speed front end (HSFE) portion of the Multimegabit Telemetry Demodulator-Detector. The HSFE accepts in-phase and quadrature analog signals from the input signal conditioner. It samples them with analog-to-digital converters at a maximum rate of 64 megasamples per second. The samples are processed digitally and the integrals of  $I$ ,  $Q$  and of their crossproduct over one symbol period are supplied at symbol rate to the rest of the system.*

## I. Introduction

The purpose of the Multimegabit Telemetry project is to increase the symbol rate capability of the Deep Space Network from a maximum of 250 kilosymbols per second (ksps) to a range of symbol rates between 125 ksps to 32 msp.

A demodulator-detector which operates as a suppressed carrier Costas loop receiver is currently being developed at JPL. This article describes the high speed front end (HSFE) portion.

The HSFE accepts in-phase ( $I$ ) and quadrature ( $Q$ ) analog signals from the input signal conditioner described in Ref. 1 and samples them using high-speed arithmetic operations with the sampled values as described in Ref. 2.

The results of this fast processing are supplied to the rest of the system at the symbol rate. The signals which are supplied include the integrals of  $I$ ,  $Q$  and of  $\text{sgn}(I) \times Q$  over one symbol period and the symbol phase error samples. The digitally performed integral of  $I$  over one symbol period is the soft quantized output of the system and is equivalent to an analog "integrate and dump" output.

## II. System Description

Figure 1 is the block diagram of the HSFE. The  $I$  and  $Q$  signals are sampled by the converters  $A/D_1$  and  $A/D_2$  respectively. Each of them consists of two four-bit monolithic quantizers manufactured by Advanced Micro Devices, Inc. (AM 6688).

The two quantizers are clocked at half the desired sampling rate with 180 degrees phase shifted clocks. This gives more time for data processing by the accumulators,  $ACC_1$ ,  $ACC_2$ ,  $ACC_3$ ,  $ACC_4$  and  $ACC_5$ , the squarers  $SQ_1$  and  $SQ_2$  and the multiplier  $MULT_1$ .

The  $I$  and  $Q$  signals are sampled  $K$  times during one symbol period, where  $K$  can be selected to be 2, 4, 8 or 16. At the highest data rate of 32 msp,  $K$  has to be 2, but as the rate is reduced  $K$  can be increased, provided the sampling rate does not exceed 64 MHz.

A 64-MHz sampling rate means 32 MHz for the individual quantizers, which allows just 30 ns for arithmetic operations (accumulation, squaring, sign inversion, etc.). The  $I$  channel samples are accumulated by  $ACC_1$ , which supplies the integral

of  $I$  over a one-symbol period. The same samples are squared by  $SQ_1$  and the squares are accumulated by  $ACC_2$ .

The  $Q$  channel is processed in the same way. The sums:

$$\sum_{i=1}^k I_i^2 \text{ and } \sum_{i=1}^k Q_i^2$$

are used for lock detection.

The amplitudes of the  $I$  and  $Q$  signals are proportional to  $\cos \theta$  and  $\sin \theta$ , respectively, where  $\theta$  is the carrier phase, but the polarity is symbol-dependent.

Phase information of the carrier is obtained by multiplying  $Q$  and  $\text{sgn}(I)$ . This results in an output crossproduct proportional to  $\sin \theta$  having the right polarity.

There are two modes of operation: acquisition and tracking. During carrier acquisition the crossproduct is calculated by  $MULT_1$  using the  $Q$  samples and the sign of the  $I$  samples. The products are accumulated over one sample period by  $ACC_5$ .

When the system switches to tracking, the signal to noise ratio is increased by using the crossproduct of

$$\sum_{i=1}^k Q_i$$

and the sign of

$$\sum_{i=1}^k I_i.$$

This product is calculated by  $MULT_2$ . Switching between acquisition and tracking is done by the multiplexer  $MUX_1$  according to the condition of the IN LOCK DETECTOR.

The HSFE also detects symbol transitions and the transition output TR is "1" for one symbol period following a transition. This information is accumulated and used for loop parameter control. Another function of the HSFE is to supply the symbol phase necessary for symbol lock. This is done by sampling the  $I$  input at transition time with  $A/D_3$ , which consists of a single four-bit quantizer.

The symbol phase samples are multiplied by  $MULT_3$  with +1 or -1 depending upon the symbol transition polarity or

with zero when no transition has taken place. The symbol phase information is supplied at the phase output.

### III. Hardware Description

Since data must be processed at maximum rates of 32 MHz and some functions of the circuit are clocked at four times this rate, it was necessary to use emitter coupled logic (ECL) integrated circuits. The circuits used are mostly MECL 10,000 and some higher speed MECL III.

The 10,000 series has by design slower transitions at the outputs, while internally the propagation delays and transitions are kept very short. This allows the user to avoid stripline techniques when not absolutely necessary because of the reduced crosscoupling.

ECL circuits require a ground plane, a -5.2 V power plane and a -2 V power plane for the terminating resistors. Special boards are made for wire-wrapping ECL. They have pins 1 and 16 grounded on the board as required in order to avoid oscillations. For this development though, it was considered economical to use standard wire-wrap boards since all the hardware was already available for them. Standard wire-wrap boards have only two planes, so the -2 V plane was avoided by using Thevenin equivalent terminators.

In order to eliminate parasitic oscillations, ferrite beads were placed on pin 1 of most of the ECL circuits. Twisted pairs with the associated line drivers and receivers were used for long connections on board or between boards. The system was divided into four main boards:

- A — The converter and clock board
- B, B' — The  $I$  and  $Q$  channel processing boards
- C — The crossproduct board

Board A generates the clocks according to the  $K$  input and distributes them to the other boards of the HSFE and to the rest of the system. It also accepts the  $I$  and  $Q$  channels from the input signal conditioner and contains the five quantizers which convert the two signals digitally.

Boards B and B' are identical. They contain the accumulators and the squarers which perform  $I$ ,  $Q$ ,  $I^2$ ,  $Q^2$ . Board C contains the crossproduct multipliers and accumulators, the transition detectors, and the symbol phase circuits.

The quantizers used in board A require very short pulses and are sensitive to interference from the rest of the digital circuits. Therefore, decoupling components are very closely

connected. This excludes wire wrapping from the quantizer portion of the board. In this area, the wire-wrap board is cut out and a double-sided board is substituted. This board contains the quantizers and associated components as shown in Fig. 2. The ground and power planes were soldered at the junction in order to keep plane continuity. This permits ECL interconnections to be made with "wire above ground" transmission lines and avoids interruptions in the ground plane which would lead to waveform distortion.

#### IV. Testing of the Hardware

The hardware was tested in two steps. The converter and clock board was tested first. The digital signal processing boards (B, B' and C) were tested independently of the converter and clock board. The reason for this two-step testing procedure is that it is very difficult to generate analog signals with predetermined values when sampled at a maximum frequency of 64 MHz.

##### A. Testing of Board A (Converter and Clock)

The test setup is shown in Fig. 3.  $I$  and  $Q$  are the in-phase and quadrature inputs. CK is the clock input, which can be as high as 128 MHz.  $C_s$  is the symbol clock, which is distributed to the digital processing part of the system; it can be as high as 32 MHz.  $C_2$  is the sampling clock, it is distributed just to the high speed front end portion of the system, and it has one-fourth the frequency of CK.

The board has five digital outputs:  $I/C_1$ ,  $I/C_2$ ,  $I/C\phi$ ,  $Q/C_1$ ,  $Q/C_2$ . They are the 4-bit values of the  $I$  and  $Q$  inputs, sampled by the five analog-to-digital converters of the board synchronous with the internal clocks  $C_1$ ,  $C_2$  and  $C\phi$ . The test setup consists of three synchronized synthesizers (SYNTH 1, SYNTH 2 and SYNTH 3), a power splitter (PS), two 4-bit registers (Reg 1, Reg 2), two digital-to-analog converters ( $D/A_1$ ,  $D/A_2$  — computer labs HDS-0810E, 100-MHz converter) and an oscilloscope. The two registers can be connected to any of the five 4-bit outputs of Board A.

The sinewave output of SYNTH 1 is split by the PS and fed to the  $I$  and  $Q$  inputs. Its frequency is  $f_1$ . SYNTH 2 supplies the clock input CK with  $f_2$ , and SYNTH 3 triggers the oscilloscope externally at a frequency  $f_3$ . We set  $f_1 = 32.001$  MHz,  $f_2 = 128$  MHz and  $f_3 = 1$  kHz. All three signals are coherent because SYNTH 2 and SYNTH 3 are synchronized from SYNTH 1.

The frequency of  $C_2$  is one-fourth that of CK; therefore, the signal is sampled at  $f_2 \div 4 = 32$  MHz. Since the frequency of  $I$  and  $Q$  is  $f_1 = 32.001$  MHz, the output samples  $I/C_1$  through  $Q/C_2$  will have a periodicity of 1 kHz.

The samples are strobed by Reg 1 and Reg 2 and then converted to 1-kHz sinewaves by  $D/A_1$  and  $D/A_2$ , which can be observed on the oscilloscope triggered by SYNTH 3 at  $f_3 = 1$  kHz.

This method allows testing of the analog-to-digital converters from two points of view at the same time; we can see the frequency response of the input stage of the A/D and whether the sampling frequency of the A/D is within the allowable range. Observing two channels at the same time allows us to see if the sampling clocks are in the correct phase relationship.

The board was tested and found to work well for full-scale sinewave inputs of 32 MHz and clock inputs exceeding 128 MHz.

##### B. Testing of the Digital Processing Boards (B, B', C)

The testing of the B, B', and C boards is done by substituting the digital signals from Board A with preprogrammed bit patterns from a word generator. The test setup is shown in Fig. 4.

The word generator supplies two 4-bit inputs to the digital processing boards. It also has a strobe output which marks the beginning of a symbol. Since the High Speed Front End generates its own clocks, including the symbol clock  $C_s$ , it was necessary to synchronize the strobe signal with the symbol clock from Board A. This was done by means of a phase-locked loop. The strobe output and the symbol clock phases are compared by the phase-sensitive detector PSD (MC 12040). The phase error controls a synthesizer in the search mode, which acts like a voltage-controlled oscillator (VCO). This VCO triggers a pulse generator which supplies the input clock CK to Board A. The delay line (DL) delays the digital outputs from the word generator approximately 14 ns relative to the symbol clock. This duplicates the conditions that exist when signals generated by Board A are used as input. A switching arrangement allows checking of all five inputs.

By feeding known bit patterns at various rates it was possible to extensively check the logic design, the wiring and the working speed. It was found that the system performs correctly at sample rates in excess of 32 MHz.

#### V. Summary

The HSFE has been constructed and tested. It supplies other parts of the Multimegabit Telemetry System and the user with digital signals through differentially driven, shielded, twisted pairs with an impedance of 120  $\Omega$ . The clock supplied with the data is advanced 24 ns, which allows the clock to be distributed throughout the system with no difficulty.

## References

1. Stevens, G. L., "Input Signal Conditioner for the Multimegasymbol Telemetry System Feasibility Model," in *The TDA Progress Report 42-58*, May-June 1980, Jet Propulsion Laboratory, Pasadena; Calif., Aug 15, 1980.
2. Wechsler, E. R., "Arithmetic Techniques Used in the High Speed Front End of the Multimegabit Telemetry Modem," in *The DSN Progress Report 42-56*, January-February 1980, Jet Propulsion Laboratory, Pasadena, Calif., April 15, 1980.



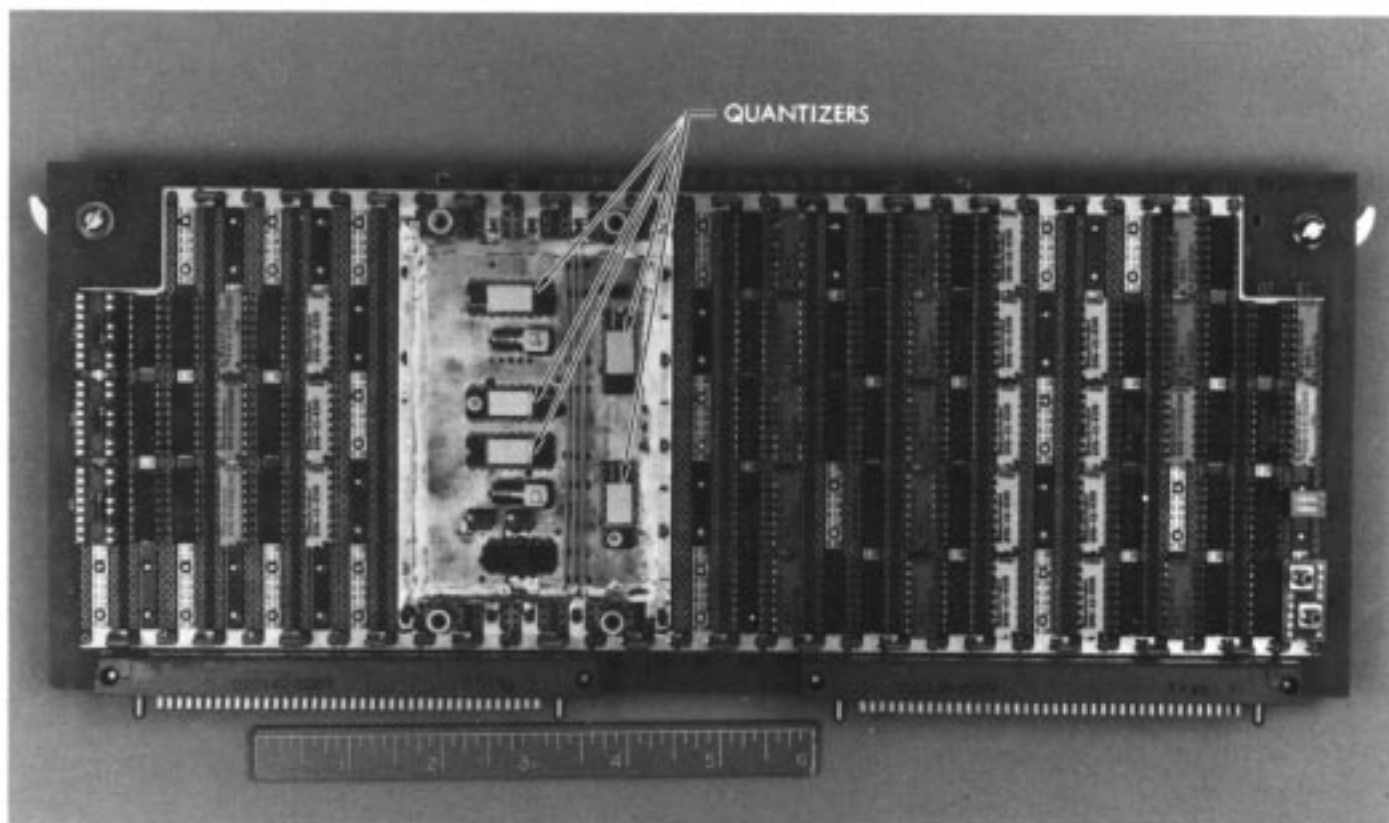


Fig. 2. Converter and clock board

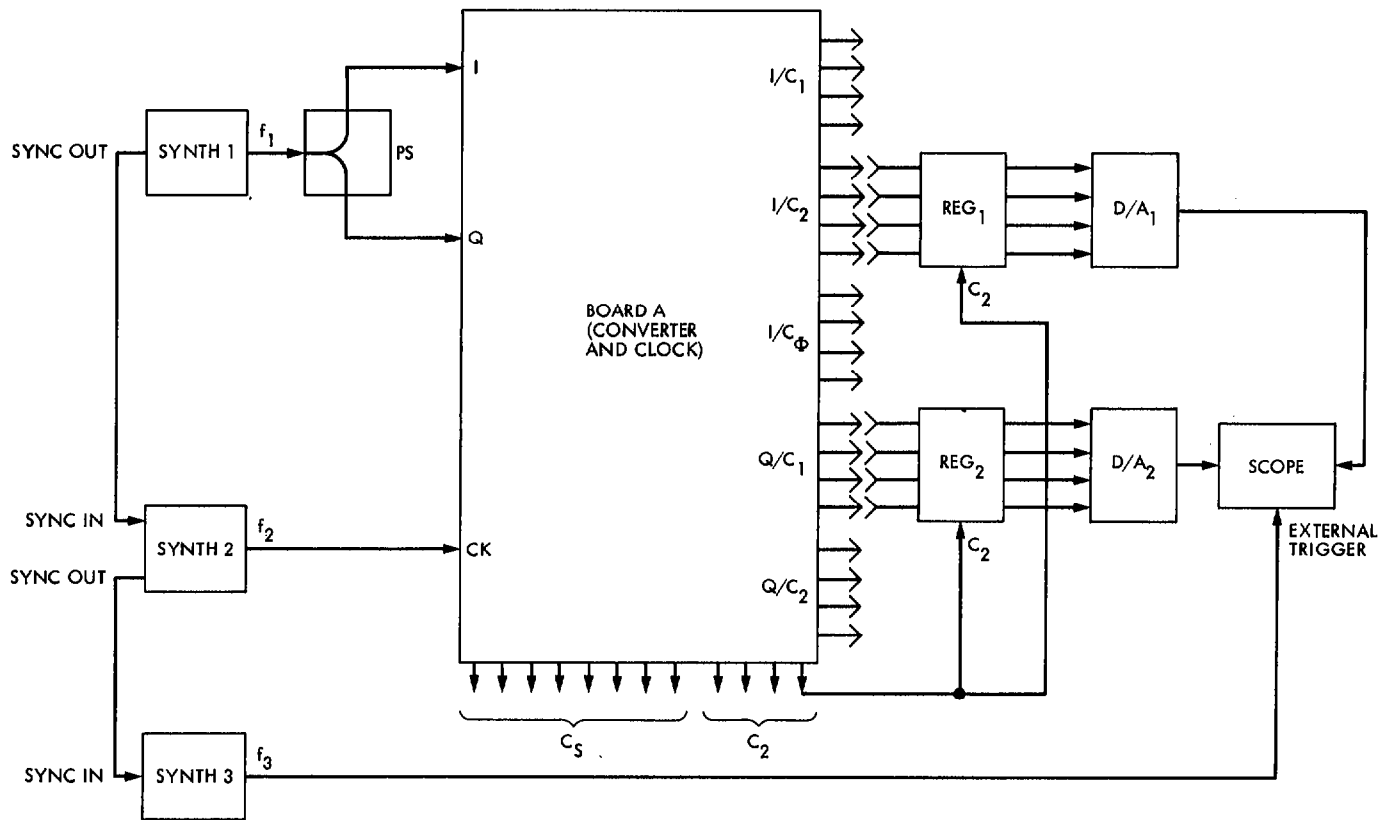


Fig. 3. Test setup for the converter and clock board

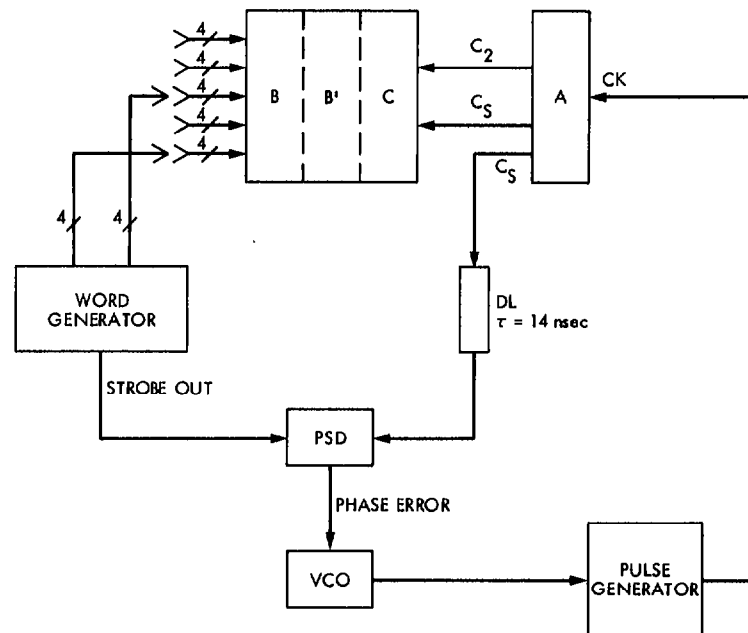


Fig. 4. Testing of the digital signal processing boards (B, B', C)